IFW AF 2811

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	**Confirmation No. 4745**
Tomoji HAMADA	:	Docket No.2003_0996A
Serial No. 10/623,655	:	Group Art Unit 2811
Filed July 22, 2003	:	Examiner J. M. IM
SEMICONDUCTOR APPARATUS	:	**Mail Stop: AF**

REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37. CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2811

Sir:

Responsive to the Office Action mailed March 25, 2005, please consider the following remarks.

In the final rejection mailed March 25, 2005, claims 1, 11, 13-15 and 17-19 were rejected under 35 U.S.C. §102(b) as being anticipated by Hung et al.; claims 2, 3, 6 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hung et al. in view of Karnezos; claims 4, 5, and 8-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hung et al. and Karnezos, and further in view of Adachi et al.; and claims 12 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hung et al. in view of Adachi et al. These rejections are respectively traversed for the following reasons.

Initially, the courtesies extended by Examiner Im during telephonic interview conducted on June 21, 2005 are greatly appreciated. During this telephonic interview, Examiner Im more clearly explained how claim 1 is being read on Hung et al. with regard to the semiconductor device being connected with the external electrodes via the first through-hole wiring and the internal wiring.

Irrespective of the position taken by the Examiner as expressed during this interview, it is respectfully submitted that claim 1 is not anticipated by Hung et al. for the following reasons.

Claim 1 recites a semiconductor apparatus that comprises *inter alia* external **electrodes**. In rejecting claim 1 as being anticipated by Hung et al., the Examiner equated reference numeral 216 to the claimed external electrodes; however, reference numeral 216 refers to a conductive layer. Accordingly, even though reference numeral 216 can arguably be considered to correspond to an electrode since it is a conductive layer, it is respectfully submitted that it is not reasonable to construe this single conductive layer 216 as more than one electrode, as is required by claim 1. Thus, for this reason claim 1 is not anticipated by Hung et al.

Adachi et al. and Karnezos do not resolve this deficiency of Hung et al., and accordingly, claim 1 is allowable over any possible combination of the references relied upon by the Examiner.

Similarly, claims 18 and 19 are believed to be patentable in their own right because these claims require that of the plural electrodes of claim 1, one is an electrode for grounding. In rejecting claims 18 and 19, the Examiner directed Applicant's attention to column 5, lines 24-46 of Hung et al. This portion of Hung et al., along with Hung et al. in its entirety, has been studied, and it is not seen how this reference discloses plural electrodes with one of these electrodes being an electrode for grounding.

If the Examiner continues to reject claim 1 as being anticipated by Hung et al., then the Examiner is respectfully requested to specifically explain how this reference teaches the electrodes as required by claim 1.

Additionally, claim 16 is believed to be patentable in its own right because it recites a limitation that is not taught or suggested by any combination of the references relied upon by the Examiner. In this regard, claim 16 requires a metal plate having the semiconductor device mounted thereon, wherein the external electrodes and the metal plate are co-planar. In finding claim 16 to have been obvious to one having ordinary skill in the art, the Examiner relied upon a combination of Hung et al. and Adachi et al. Specifically, the Examiner expressed that in view of lead 11C and bed portion 12C being co-planar as shown in Figure 6, one would have found it obvious to have the external electrodes and metal plate 202 of Hung et al. be co-planar so as to reduce a package size. This position is respectfully traversed for the following reasons.

Assuming arguendo that one sought to reduce the package size of Hung et al. and that conductive layer 216 corresponds to electrodes, the apparent ways to reduce the package size would be to either eliminate layers 210-226 such that the base 202 supports conductive layer 216, or eliminate base 202 along with layers 210-226. In any event, the package of Hung et al., after being reduced in package size, would not include base 202 being coplanar with conductive layer 216. In this regard, the base 202 would either be beneath conductive layer 216, or would not be present at all.

To modify Hung et al. as suggested by the Examiner such that claim 16 reads on a combination of Hung et al. and Adachi et al., a portion of conductive layer 216 would have to be replaced by a portion of base 202. It is respectfully submitted that there is no suggestion in any of the relied-upon references to modify Hung et al. in such a manner, and it is only through impermissible hindsight that such a modification is even contemplated. Thus, claim 16 is patentable in its own right.

Claims 1-19 are allowable.

In view of the above amendments and remarks, it is respectfully submitted that the present application is in condition for allowance and an early Notice of Allowance is earnestly solicited.

If after reviewing this Amendment, the Examiner believes that any issues remain which must be resolved before the application can be passed to issue, the Examiner is invited to contact the Applicant's undersigned representative by telephone to resolve such issues.

Respectfully submitted,

Tomoji HAMADA

By: Joseph M. Gorski

Joseph M. Gorski
Registration No. 46,500
Attorney for Applicant

JMG/kjf
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
June 27, 2005